In the Claims:

Please amend the claims as follows:

1-33 (cancelled)

34. (new) A method for manufacturing electronic thin-film components, said method comprising:

selecting a substantially dielectric substrate;

forming a lowermost, galvanically uniform conductive layer of an electrically conductive material on said substrate;

galvanically separating conductive areas from each other from said lowermost conductive layer to form an electrode pattern by exerting on the lowermost conductive layer a machining operation based on die-cut embossing, wherein the relief of the machining member used in the machining operation causes a permanent deformation on the substrate and at the same time embosses areas from the conductive layer into conductive areas galvanically separated from each other, said conductive areas being on at least two different levels, which levels have different positions in a direction perpendicular to the plane of the substrate; and

forming one or several upper layers required in the thin-film component on top of said electrode pattern.

35. (new) The method according to claim 34, wherein by means of said embossing operation exerted on the lowermost conductive layer, one or more upper layers of the thin-film

component are formed simultaneously.

36. (new) The method according to claim 34, wherein the lowermost conductive layer formed on the substrate, which is to be patterned by means of embossing, is produced by vacuum coating.

37. (new) The method according to claim 36, wherein said vacuum coating and embossing are performed in the same vacuum process.

38. (new) The method according to claim 34, wherein said dielectric substrate is selected from a group consisting of plastic, glass, paper, paperboard, and a laminated combination thereof.

39. (new) The method according to claim 38, wherein the substrate material is heated for the embossing.

40. (new) The method according to claim 39, wherein when the substrate material contains plastic, the embossing of said lowermost conductive layer is performed at a temperature, which is slightly above the glass transition temperature of said plastic material.

41. (new) The method according to claim 34, wherein the material of the lowermost conductive layer is selected from a group consisting of transparent semiconducting oxide, non-transparent semiconducting oxide, metal, conductive ink, conductive polymer, and a combination

thereof.

42. (new) The method according to claim 34, wherein the vertical depth of the machining member used in embossing is selected from the range of 1 to 50 μm.

43. (new) The method according to claim 34, wherein the horizontal line widths used in the embossing are selected from the range of 1 to 50 μm.

44. (new) The method according to claim 34, wherein the relief of the machining member used in the embossing is selected so that it has substantially upright walls in the vertical direction.

45. (new) The method according to claim 34, wherein a nickel pressing block or plate is used as the machining member in the embossing, the relief of the master of said plate being formed by means of direct resist lithography.

46. (new) The method according to claim 34, wherein a nickel pressing block or plate is used as the machining member in the embossing, the relief of the master of said plate being formed by a combination of resist lithography and dry etching technique.

47. (new) The method according to claim 34, wherein several process stages are performed in the same roll-to-roll process.

48. (new) The method according to claim 34, wherein the electrode pattern formed by means of embossing or the upper passive or active layers formed simultaneously by means of embossing are post-treated by means of a plasma processing.

49. (new) An apparatus for manufacturing electronic thin-film components on a substantially dielectric substrate, said apparatus comprising:

first growing means for growing a lowermost, galvanically uniform conductive layer of an electrically conductive material on said substrate;

patterning means for galvanically separating the conductive areas from each other from said lowermost conductive layer to form an electrode pattern, said patterning means being embossing means based on die-cut embossing, said means comprising at least one machining member whose relief causes a permanent deformation on the substrate and at the same time embosses areas from the conductive layer into conductive areas galvanically separated from each other, said patterning means being arranged to form said conductive areas by said embossing operation such that said conductive areas are on at least two different levels, which levels have different positions in a direction perpendicular to the plane of the substrate; and

second growing means for forming one or several upper layers required in a thin-film component on top of said electrode pattern.

50. (new) The apparatus according to claim 49, wherein said patterning means are arranged to form one or several upper layers of the thin-film component simultaneously by means of said embossing operation exerted on the lowermost conductive layer.

51. (new) The apparatus according to claim 49, wherein said first growing means for forming the lowermost conductive layer to be patterned by means of embossing on the substrate are vacuum coating means.

52. (new) The apparatus according to claim 51, wherein said vacuum coating means and embossing means are arranged in the same vacuum process.

53. (new) The apparatus according to claim 49, wherein the vertical depth of the relief of the machining member used in embossing is in the range 1 to 50 μm.

54. (new) The apparatus according to claim 49, wherein the relief of the machining member used in the embossing is arranged so that it has substantially upright walls in the direction perpendicular to the plane of the substrate.

55. (new) The method according to claim 49, wherein the machining member used in the embossing is a nickel pressing plate, the relief of the master of said machining member being formed by means of a combination of resist lithography and dry etching technique.

56. (new) The apparatus according to claim 49, wherein at least said first growing means and said patterning means are arranged to be in the same roll-to-roll process.

57. (new) An electronic thin-film component, comprising:

a substantially dielectric substrate;

a lowermost conductive layer of an electrically conductive material formed on said substrate, wherein said conductive layer is patterned into conductive areas galvanically separated from each other and forming an electrode pattern by exerting on the lowermost conductive layer a machining operation based on die-cut embossing, wherein the relief of the machining member used in the machining operation causes a permanent deformation on the substrate and at the same time embosses areas from the conductive layer into conductive areas separated from each other galvanically, said conductive areas being on at least two different levels, which levels have different positions in a direction perpendicular to the plane of the substrate; and

one or several upper passive or active layers formed on top of said electrode pattern.

58. (new) The component according to claim 57, wherein the component comprises one or several upper layers, which are formed by the same embossing operation exerted on the lowermost conductive layer.

59. (new) The component according to claim 57, wherein the material of said substrate is selected from a group consisting of plastic, glass, paper, paperboard and a laminated combination thereof.

60. (new) The component according to claim 57, wherein the material of the lowermost conductive layer is selected from a group consisting of transparent semiconducting oxide, non-transparent semiconducting oxide, metal, conductive ink, conductive polymer, and a combination thereof.

61. (new) The component according to claim 57, wherein the distance between the electrode patterns in the direction perpendicular to the plane of the substrate is in the range of 1 to 50 μm.

62. (new) The component according to claim 57, wherein the component comprises at least one upper active layer formed on top of said electrode pattern, the material of said layer being an organic or inorganic semiconducting material.

63. (new) The component according to claim 62, wherein said at least one upper active layer is arranged to form a structure selected from the group of a channel structure of a transistor, a photoactive layer of a solar cell, a photocell, and an electroluminescent layer of a light-emitting component.

64. (new) The component according to claim 57, wherein the component is selected from the group of a light emitting diode, a field effect transistor, an active or passive pixel display, a photocell,and a solar cell.

65. (new) The component according to claim 57, wherein the component comprises one or more upper layers, whose perpendicular dimension with respect to the plane of the substrate is determined by the embossing operation exerted on the lowermost conductive layer.

66. (new) The component according to claim 65, wherein the component is an organic field effect transistor OFET, the length of whose channel structure is determined by embossing

in the direction perpendicular to the plane of the substrate.

67. (new) The component according to claim 57, wherein the component is a pixel display based on organic light emitting diodes OLED, in which individual pixels of the display are formed in the intersections of crossing stripe-like electrodes representing different polarities, and in which component parallel adjacent electrodes representing the same polarity are formed on different levels with respect to the substrate in the direction perpendicular to the plane of the substrate.

68. (new) The component according to claim 57, wherein the distance between said parallel adjacent electrodes representing the same polarity is in the range 1 to 5 μm, said distance being in the direction perpendicular to the plane of the substrate.